1/4

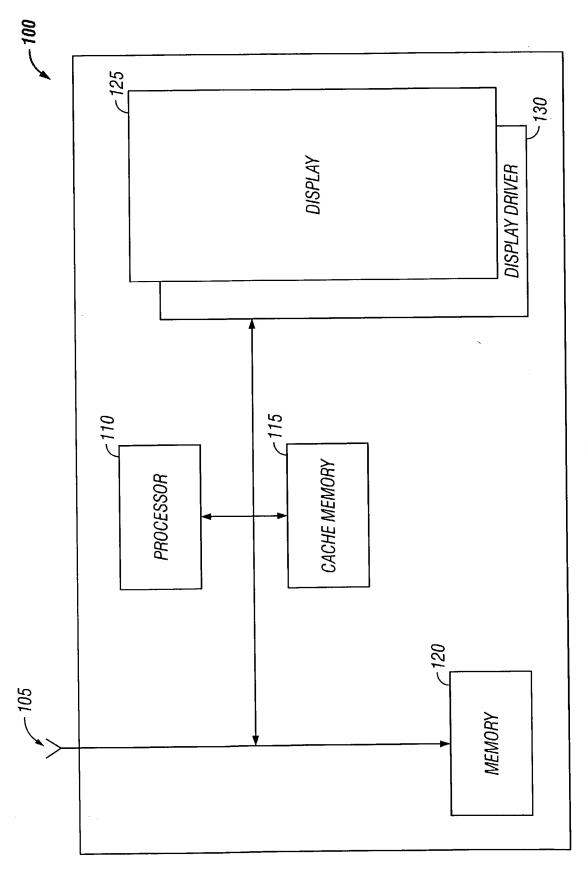
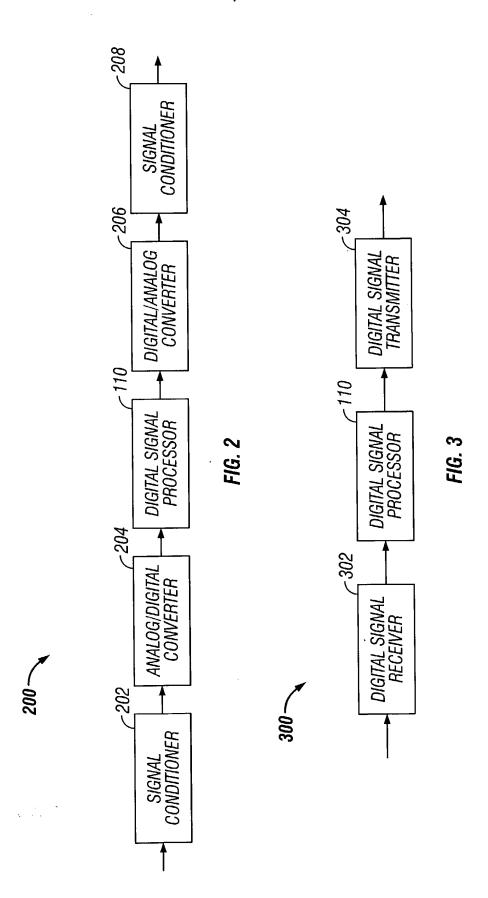


FIG. 1

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DIGITAL SIGNAL PROCESSOR WITH MULTIPLE INSTRUCTION DESTINATIONS FOR A PIPELINED SYSTEM

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09/675,816

10559-270001

	IF1	IF2	DEC	AC	EX1	EX2	EX3	WB	
1	i				_				
2	i+1	i							
3	i+2	i+1	i						
•••	•••	i+2	i+1	•••					
•••	•••	•••	i+2	•••	•••				
n	i+(n-1)	• • •	• • •	•••	•••	•••			

- CLOCK CYCLE

FIG. 4

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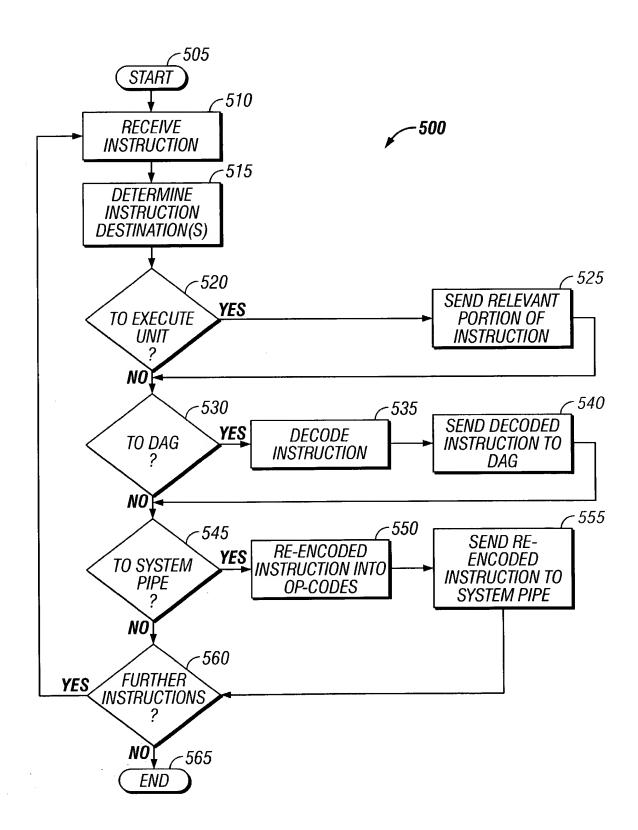


FIG. 5